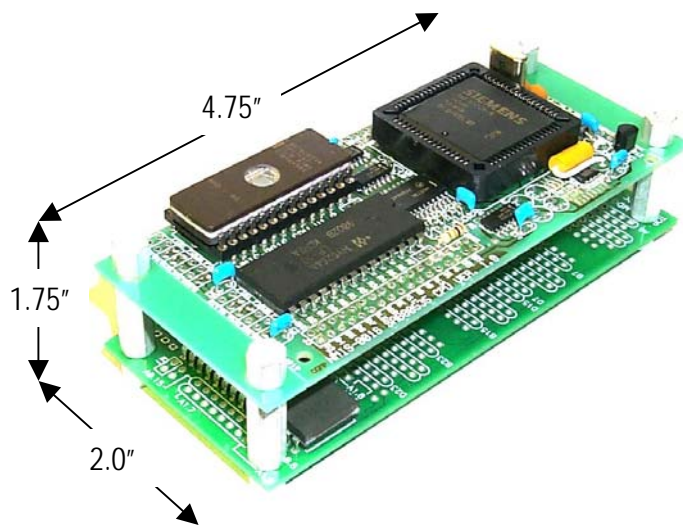


Colorado Space Grant Consortium Citizen Explorer 1 Mission

Command and Data Handling System (CDH) Micronet processor fact sheet



System configuration as flying on CX-1:

MPU (Micro-Processing Unit)	Siemens SAB 80C535 (8051-compatible)
Speed	11MHz
RAM	8KB (24KB max)
ROM	8KB (32KB max)
Digital Inputs/Outputs	19 available TTL lines each line configured as input or output
Analog Inputs	38 lines, 0-5V, 8-bit resolution
Serial	One RS485 port with TX/RX switching
Power Consumption	0.5W total +5V @ 90mA (0.45W) +15V @ 2mA (0.03W) -15V @ 1mA (0.015W)
Temperature range	-40 to +85°C
Volume	4.75" X 2.0" X 1.75"
Mass	0.5 Kg*
Cost	\$250 approximate

The Citizen Explorer Micronet processor is a small computer programmed to perform I/O functions when commanded by another computer. This processor is designed to be embedded into other spacecraft subsystems, simplifying integration and testing, and enhancing the control available to the flight computer.

The core of the microcontroller is an commercial-off-the-shelf MPU board. This board provides an 8051-compatible MPU, RAM, ROM, and basic I/O. This board is complemented by a Mux/Buffer board designed and built at CSGC, which expands the available I/O, and provides buffering and driving for all inputs and outputs.

The Micronet firmware provides a simple protocol by which many Micronet processors may listen to a single RS485 twisted pair. When a Micronet processor recognizes a command addressed to itself, it parses the command, carries out the requested I/O, and responds to the main computer. In order to prevent message collisions, all Micronet processors are configured to "not speak until spoken to", and cannot initiate communications on their own. The microne RS485 bus runs at 9600 baud. The maximum bus throughput is on the order of 10 commands / second.

The Micronet processor is not radiation-hardened. An external EPROM is used for storing firmware code, as opposed to the FLASH memory used by many microprocessors. The processor is protected against less-serious errors by an internal watchdog timer. More serious errors may be cleared by a power-cycling the processor, which can be initiated by the flight computer if a processor is not responding.

* Estimated